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SINGLE-STAGE PFC AND POWER CONVERTER CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application is based on and claims benefit of U.S. Provisional Application No. 60/450,572 filed February 27, 2003, entitled NEW SINGLE-STAGE PFC AND BALLAST CONTROL CIRCUIT/GENERAL PURPOSE CONVERTER, to which a claim of priority is hereby made and which is hereby incorporated by reference into the present application in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates generally to power converters and ballast controls with power factor correction (PFC), and relates more specifically to a single-stage power converter or ballast control that incorporates a PFC circuit.

2. Description of Related Art

[0003] Electronic ballasts and power converters that include a power factor correction (PFC) circuit are well known in the relevant industries. Typically, any type of general power converter, which includes electronic ballasts, have connected to their input a PFC circuit to preferably correct the input power factor to unity. It is desirable, and often required according to regulatory demands, that loads connected to power lines appear as purely resistive loads without any connective impedances. That is, the alternating voltage and current supplied by the line input are maintained

to be in phase with each other so that the connected load appears purely resistive. When the input voltage and current are in phase, the power factor approaches unity, thereby providing a load that appears to be purely resistive on the input line, without any apparent influence from capacitance or inductance that would otherwise occur if the voltage and current are out of phase with each other.

[0004] To achieve a unity power factor, a power factor correction circuit is typically connected to the power line input. The PFC circuit also generally produces a regulated DC bus voltage that is supplied to an inverter for use in power conversion applications. A typical power converter application is an electronic ballast for use with a fluorescent lamp. Often, an electronic ballast consists of a power inverter fed by a DC bus voltage, with the inverter being controlled to provide fluorescent lamp pre-heating, ignition and normal supply power during normal running conditions. A simple block diagram of such an application is provided in Figure 1. The electronic ballast illustrated in Figure 1 includes a half-bridge resonant output stage for powering the lamp. The PFC circuit connected to the power line input is typically realized as a boost-type converter that uses a high voltage switch, an inductor, a diode, a high voltage DC bus capacitor and a PFC control circuit. The electronic ballast output stage is typically realized with a half-bridge driven resonant load that uses two high voltage switches, a resonant inductor, a resonant capacitor, a DC-blocking capacitor and a ballast control circuit. A simplified circuit diagram of a conventional electronic ballast circuit is shown in Figure 2.

[0005] The conventional half-bridge electronic ballast output stage configuration shown in Figure 2 includes a DC bus capacitor C_{bus} that is connected across the switching half-bridge. As can be seen in the circuit diagram in Figure 2, high side half-bridge switch M1 and DC bus capacitor C_{bus} are connected together at a single node. When the conventional electronic ballast of Figure 2 is switched on, input power is first used to charge DC bus capacitor C_{bus} , which then supplies power to

the half-bridge resonant output stage while the electronic ballast operates. The PFC circuit composed of inductor L_{pfc} , switch M_{pfc} and diode D_{pfc} operate during start-up to charge bus capacitor C_{bus} . In this conventional circuit typology, power typically flows in a single direction through the load, and bus capacitor C_{bus} supplies power through the entire cycle of power transfer to the load. Accordingly, bus capacitor C_{bus} must be rated to withstand peak power transfer, and switches M_{pfc} , $M1$ and $M2$ must also be rated to withstand high peak bus voltages.

[0006] It would be desirable to reduce the ratings needed to realize a power converter circuit with an input PFC circuit, and simplify the circuit at the same time.

SUMMARY OF THE INVENTION

[0007] The present invention provides a single stage PFC and power converter for general purpose power supply for resonant loads. By modifying the circuit topology of the conventional half-bridge power converter, the present invention achieves efficiencies and reduced part counts that are improved over the conventional design. The inventive circuit configuration also reduces the requirements for component ratings so that circuit size and power consumption are reduced. The single stage power converter and PFC circuit has the potential to obtain soft switching in all switches, thereby reducing switching losses and further reducing power consumption.

[0008] In accordance with the present invention, the conventional boost converter for power factor correction is eliminated because the function is combined into the operation of supplying constant power to the load. The circuit obtains a power factor that is close to unity while providing bi-directional power flow control. A switching half-bridge is connected to the rectified line input voltage, which

permits the conventional input inductor to be omitted, while reducing the rating requirements for a DC bus capacitor. By appropriately controlling the switches in the power converter, a sinusoidal current is drawn from the line input to obtain a high power factor. In the conventional power converter, the capacitor in the boost converter was operated to maintain constant voltage over varying load and input conditions, and was thus very large. In the present invention, the boost converter is eliminated and the bus capacitor need not maintain a constant voltage, but rather serves as an energy storage device for transferring power between the input and the load. Accordingly, the bus capacitor can be reduced by a factor of up to 2-4 times.

[0009] Conduction angles for the various switches are derived to achieve constant load power while maintaining a high power factor. In addition, total harmonic distortion of the input is greatly reduced, thereby limiting radiated and conducted electromagnetic interference (EMI).

[0010] Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING

[0011] The present invention is described in greater detail below with reference to the accompanying drawings, in which:

[0012] Figure 1 is a block diagram of a prior art power converter with separate PFC and output stages;

[0013] Figure 2 is a simplified circuit diagram of a conventional power converter for driving a fluorescent lamp.

[0014] Figure 3 is a block diagram of a power converter according to the present invention with combined PFC and output stages;

[0015] Figure 4 is a simplified circuit diagram showing a circuit topology according to the present invention for driving a fluorescent lamp;

[0016] Figure 5 is a graph illustrating rectified line input voltage and current;

[0017] Figure 6 is a graph illustrating input power, load power and capacitor power;

[0018] Figure 7 is a graph illustrating conduction angles for switches in the power converter according to the present invention;

[0019] Figure 8 is a graph illustrating input current and voltage and bus capacitor voltage and current;

[0020] Figure 9 is a simplified circuit diagram illustrating bi-directional power flow according to the present invention;

[0021] Figure 10 is a graph and timing diagram illustrating conduction angle switching in the circuit according to the present invention; and

[0022] Figure 11 is a graph and timing diagram showing conduction angle switching according to the power converter of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0023] Referring now to Figure 3, a block diagram of the single stage power converter with power factor correction (PFC) is illustrated as block 30. The single

stage power converter is illustrated as driving a load, such as a resonant load for an electronic lamp ballast that powers a fluorescent lamp 32.

[0024] Referring now to Figure 4, the circuit diagram of the single stage power converter according to the present invention is illustrated generally as circuit 40. Circuit 40 includes a switching half-bridge composed of switches M1 and M2, which is connected to a simple RCL ballast resonant output stage composed of inductor L, capacitor C, DC capacitor CDC and lamp 32. Switches M1 and M2 are operated in complementary fashion, that is, both switches are not on at the same time. In addition, when switches M1 and M2 are turned on and off in sequence, a dead time is introduced in between the switching sequence to avoid short circuit conditions. An exemplary dead time is approximately two microseconds. A switch M3 connects a DC bus capacitor CBUS to the central node of the switching half-bridge. Circuit 40 differs from conventional electronic ballast circuit 20 shown in Figure 2 by employing a single inductor L and reducing the capacitance requirements for capacitor CBUS. By reducing the rating requirements for capacitor CBUS, a non-electrolytic type capacitor may be used in the circuit to reduce cost and improve reliability of the electronic ballast.

[0025] The resonant network may also be replaced by a piezoelectric transformer equivalent, and the lamp may also be replaced by a transformer coupled resistive load in the case of an AC to DC converter. Accordingly, the circuit of the present invention is also suitable for use as a general purpose converter with power factor correction and reduced cost and component count.

[0026] Electronic ballast circuit 40 obtains bi-directional power flow through the load when connected as illustrated. The load receives power from the rectified line input, for example, when the rectified line input voltage is high, through the switching half-bridge, and is also supplied power from the bus capacitor CBUS when

the rectified line input voltage is low. In this configuration, capacitor CBUS supplies power for a portion of the input line voltage cycle, rather than over the entire input cycle, as is the case in conventional circuit 20 in Figure 2. Switches M1, M2 and M3 are controlled to draw a sinusoidal current from the line input to obtain a high power factor. The circuit configuration obtains an advantageous total harmonic distortion (THD) on the input as well. The half-bridge obtains this advantage for the input without resorting to a boost circuit that would otherwise be carefully controlled to reduce THD to acceptable levels. In addition, control of switches M1, M2 and M3 maintains a charge on bus capacitor CBUS, and provides constant power to the load. In this configuration, the resonant output stage consists of inductor L, capacitor C, lamp 32 and DC bus capacitor CBUS.

[0027] The topology of circuit 40 is configured to operate so that each switch has a particular function. For example, switch M1 supplies current to the resonant lamp load from the rectified line input, and is switched on and off to draw sinusoidal current from the line input to achieve a high power factor. Switch M2 is switched on and off to obtain a recirculation path in circuit 40 to maintain bi-directional current flow in the resonant circuit. Switch M3 operates to charge DC bus capacitor CBUS when the line input voltage is high, and supplies current to the load when the line input voltage is low, to maintain constant power supplied to the load. It is possible to configure the operation of switches M1-M3 so that soft switching occurs in each switch. Switch turn on/turn off operation is configured according to a particular curve in this instance to avoid hard, or non-zero voltage switching for each of the switches.

[0028] Circuit 40 obtains a high power factor that approaches unity because the input line voltage and current are controlled to be sinusoidal and in phase with each other. With this high power factor, circuit 40 appears as a resistive load to the line input voltage, thereby reducing impedances on the line input and meeting

requirements under regulatory standards. Referring now to Figure 5, the rectified line input is presumed to be the output of a full bridge rectifier to achieve full wave rectification. Figure 5 illustrates the full wave rectified voltage and current being in phase with each other, as is typically the case in a standard or close to ideal full wave rectifier. In this instance, the input power is determined by multiplying the input voltage and current together. Equation 1 gives the expression of the input power.

$$P_{input} = P_{load} (1 - \cos 2\theta) \quad (1)$$

[0029] If the goal of the converter is to supply constant power to the load, the power supplied by bus capacitor CBUS is determined by subtracting the load power from the input power and is expressed in equations 2 and 3.

$$P_{capacitor} = P_{load} - P_{input} \quad (2)$$

$$P_{capacitor} = P_{load} - P_{load} (1 - \cos 2\theta) = P_{load} \cos 2\theta \quad (3)$$

[0100] Referring now to Figure 6, a graph illustrating input power, load power and capacitor power over a complete cycle of the line input voltage is provided. Note how the capacitor power changes with the input power to maintain a constant load power.

[0101] To achieve the design goal of constant load power, the conduction angles of switches M1 and M3 are determined. Conduction angle α for switch M1 and β for switch M3 are solved with respect to a complete load current cycle, which tends to be at a much higher frequency than the line input frequency. Conduction angle α is determined using the relationship between the instantaneous line input current and the average high frequency load current and is expressed below in equations 4-6.

$$\alpha = \alpha_1 \text{ when } \beta < 0, \text{ or, } \alpha = \alpha_2 \text{ when } \beta \geq 0 \quad (4)$$

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$$\alpha_1 = \frac{360}{2\pi} \left\{ \arccos \left(\frac{-2 \cdot \pi \cdot P_{in}}{V_{in} \cdot i_{load}} + 1 \right) \right\} \quad (5)$$

$$\alpha_2 = \frac{360}{2\pi} \left\{ \arccos \left(-2 \cdot \pi \cdot \left| \frac{P_{in}}{V_{in} \cdot i_{load}} \right| + \cos \left(\beta \cdot \left(\frac{2 \cdot \pi}{360} \right) \right) \right) \right\} \quad (6)$$

[0102] Conduction angle β is determined using the relationship between the capacitor power and the average high frequency load current and is expressed below in equation 7.

$$\beta = \frac{360}{2\pi} \left\{ \arccos \left(-2 \cdot \pi \cdot \left| \frac{P_{Cbus}}{V_{Cbus} \cdot i_{load}} \right| + 1 \right) \right\} \cdot \text{sign} \left(\frac{P_{Cbus}}{V_{Cbus} \cdot i_{load}} \right) \quad (7)$$

[0103] Referring now to Figure 7, a graphical representation of conduction angles α and β is presented. The graph in Figure 7 illustrates how conduction angles α and β change dynamically over a complete cycle of the line input voltage for a typical line input voltage, load power, capacitor voltage and capacitor value.

[0104] Referring now to Figure 8, a plot of input voltage and current is illustrated superimposed upon plots of current and voltage for bus capacitor CBUS. The illustrated voltages and currents are provided for a typical input voltage and load power.

[0105] Conduction angles α and β are used to turn on and off switches M1, M2 and M3 for particular times and durations during each high frequency load current cycle, based on values for α and β during each low frequency cycle of the input line voltage. The conduction angle for each switch is summarized in Table I below.

TABLE I

Switch	$\beta \geq 0$	$\beta < 0$
M1	From β to α_2	From 0 to α_1
M2	From 180 to β	From α_1 to 180
M3	From α_2 to 180	From 180 to 360

[0106] The conduction angles and switch operation are describe in greater detail with reference to Figures 9-11 below.

[0107] Referring now to Figure 9, a current loop diagram is illustrated showing current pathways and loops during different switching and conduction cycles. Referring to Figures 10 and 11, the occurrence and duration of each of the current paths or loops is described with reference to current load and switching cycles. For example, Figure 10 shows a corresponding on and off times for switches M1, M2 and M3 during one period of a typical resonant load current when $\beta \geq 0$. Switch M1 is turned on during the angle from β to α_2 degrees. Current i_A illustrated in Figure 9 flows from V_{in} through switch M1, through the resonant load, and back to the return ground to V_{in} . Switch M1 is then turned off and switch M3 is turned on during the angle from α_2 to 180 degrees. Current i_C flows from capacitor CBUS through switch M3, through the resonant load and back to the return ground to capacitor CBUS. Switch M3 is turned off and switch M2 is turned on from 180 to 360 degrees. Current i_D flows from the resonant load, through switch M2 and back to the return ground to the resonant load. Switch M2 remains on from 0 to β and current i_B flows from the return ground of the resonant load, through switch M2 and back to the resonant load. The cycle then repeats itself with switch M1 being turned on again.

[0108] Figure 11 illustrates the corresponding on and off times of switches M1, M2 and M3 during one period of a typical resonant load current when $\beta < 0$. Switch M1 turns on during the angle from 0 to α_1 degrees. Current i_A flows from V_{in} through switch M1, through the resonant load and back to the return ground to voltage V_{in} . Switch M1 is then turned off and switch M2 is turned on during the angle from α_1 to 180 degrees. Current i_B flows from the return ground of the resonant load, through the body diode of switch M2 and back to the resonant load. Switch M2 is then turned off and switch M3 is turned on from 180 degrees to 360 degrees. Current i_E flows from the resonant load, through switch M3, through capacitor CBUS and returns to ground at the resonant load. The cycle then repeats itself with switch M1 being turned on again.

[0109] As conduction angles α and β change during the low frequency cycle of the line input voltage, i.e., as shown in Figure 7, the conduction angles of the switches are controlled so that the average line input current is sinusoidal and in phase with the input voltage. This control scheme achieves a high power factor with a low total harmonic distortion while maintaining a constant load power. Under steady operating conditions, high frequency current flows through the resonant load at a constant amplitude by drawing load current from the line and charging bus capacitor CBUS when the input line voltage is high, drawing load current from the capacitor when the line input voltage is low, or recirculating load current when necessary.

[0110] The single stage ballast control and PFC circuit according to the present invention provides a number of advantages including the use of a single inductor and lower DC bus capacitance grading requirements. The circuit obtains a high power factor in a more efficient organization with low input current total harmonic distortion and reduced component count, size and cost for the electronic ballast/power converter.

[0111] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.